a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region.

22.

18. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region, and

a wiring formed on and in electrical contact with said first impurity region.

23. 21

19. The semiconductor memory device according to claim 18 wherein said wiring is a wordline.

20. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region; and

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region, and

a pair of wirings formed on and in electrical contact with said second and third impurity regions, respectively.

21. The semiconductor memory device according to claim 20 wherein each of said wirings is a bit line.

22. A semiconductor memory device comprising:

a semiconductor substrate;

a floating gate formed over said semiconductor substrate;

a control gate formed over and insulated from said first floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

an interlayer insulating film formed over said semiconductor substrate, said floating gate and said control gate; and

a wiring formed on said interlayer insulating film wherein said wiring is electrically connected to said second impurity region through a hole formed in said interlayer insulating film.

23. The semiconductor memory device according to claim 22 wherein said wiring is a bit line.

50-56

24. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region,

an interlayer insulating film formed over said semiconductor substrate, said first and second floating gates and said first and second control gates; and

a pair of wirings formed on said interlayer insulating film and electrically connected to said second and third impurity regions, respectively, through holes of said insulating film.

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25. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region, wherein said first impurity region is partly overlapped with said first floating gate; and

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, said first impurity region being deeper than said third impurity region, wherein said first impurity region is partly overlapped with said second floating gate.

26. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region wherein said first impurity region is partly overlapped with said first floating gate; and

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, said first impurity region being deeper than said third impurity region, wherein said first impurity region is partly overlapped with said second floating gate,

a pair of wirings formed on and in electrical contact with said second and third impurity regions, respectively.

27. The semiconductor memory device according to claim 26 wherein each of said wirings is a bit line.

28. A semiconductor memory device comprising:

a semiconductor substrate;

a floating gate formed over said semiconductor substrate;

a control gate formed over and insulated from said floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region, wherein said first impurity region is partly overlapped with said floating gate;

an interlayer insulating film formed over said semiconductor substrate, said floating gate and said control gate; and

a wiring formed on said interlayer insulating film wherein said wiring is electrically connected to said first impurity region through a hole formed in said interlayer insulating film.

90. 89.

29. The semiconductor memory device according to claim 28 wherein said wiring is a bit line.

100. 104.

30. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region and said first impurity region is partly overlapped with said first floating gate;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region, wherein said first impurity region is partly overlapped with said second floating gate;

an interlayer insulating film formed over said semiconductor substrate, said first and second floating gates and said first and second control gates; and

a pair of wirings formed on said interlayer insulating film and electrically connected to said second and third impurity regions, respectively, through holes of said insulating film.

31. The semiconductor memory device according to claim 17 wherein said device is an EPROM device.

32. The semiconductor memory device according to claim 18 wherein said device is an EPROM device.

33. The semiconductor memory device according to claim 20 wherein said device is an EPROM device.

34. The semiconductor memory device according to claim 22 wherein said device is an EPROM device.

35. The semiconductor memory device according to claim 24 wherein said device is an EPROM device.

36. The semiconductor memory device according to claim 25 wherein said device is an EPROM device.

37. The semiconductor memory device according to claim 26 wherein said device is an EPROM device.

38. The semiconductor memory device according to claim 28 wherein said device is an EPROM device.

39. The semiconductor memory device according to claim 30 wherein said device is an EPROM device.

40. The semiconductor memory device according to claim 17 wherein said device is an EEPROM device.

41. The semiconductor memory device according to claim 18 wherein said device is an EEPROM device.

42. The semiconductor memory device according to claim 20 wherein said device is an EEPROM device.

43. The semiconductor memory device according to claim 22 wherein said device is an EEPROM device.

44. The semiconductor memory device according to claim 24 wherein said device is an EEPROM device.

45. The semiconductor memory device according to claim 25 wherein said device is an EEPROM device.

46. The semiconductor memory device according to claim 26 wherein said device is an EEPROM device.

47. The semiconductor memory device according to claim 28 wherein said device is an EEPROM device.

48. The semiconductor memory device according to claim 30 wherein said device is an EEPROM device.

49. The semiconductor memory device according to claim 17 wherein said device is a flash memory device.

50. The semiconductor memory device according to claim 18 wherein said device is a flash memory device.

51. The semiconductor memory device according to claim 20 wherein said device is a flash memory device.

48. 50. 44 52. The semiconductor memory device according to claim 22 wherein said device is a flash memory device.

59. 61. 51 53. The semiconductor memory device according to claim 24 wherein said device is a flash memory device.

70. 72. 69 54. The semiconductor memory device according to claim 25 wherein said device is a flash memory device.

81. 84. 80 77 55. The semiconductor memory device according to claim 26 wherein said device is a flash memory device.

93 96. 92 89 56. The semiconductor memory device according to claim 28 wherein said device is a flash memory device.

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103 107. 104 100 57. The semiconductor memory device according to claim 30 wherein said device is a flash memory device.

15 15. 11 58. The semiconductor memory device according to claim 17 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

26. 17. 22 59. The semiconductor memory device according to claim 18 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

29. 37 34 32 60. The semiconductor memory device according to claim 20 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

60. 62. 51 61. The semiconductor memory device according to claim 24 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

71. 73. 69 57 62. The semiconductor memory device according to claim 25 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

63. The semiconductor memory device according to claim 26 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

64. The semiconductor memory device according to claim 30 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

65. The semiconductor memory device according to claim 22 wherein said floating gate comprises phosphorus doped polysilicon.

66. The semiconductor memory device according to claim 28 wherein said floating gate comprises phosphorus doped polysilicon.

67. The semiconductor memory device according to claim 17 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

68. The semiconductor memory device according to claim 18 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

69. The semiconductor memory device according to claim 20 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

70. The semiconductor memory device according to claim 24 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

71. The semiconductor memory device according to claim 25 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

72. The semiconductor memory device according to claim 26 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

73. The semiconductor memory device according to claim 30 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

74. The semiconductor memory device according to claim 22 further comprising an insulating layer formed on upper and side surfaces of the floating gate and the control gate wherein said insulating layer is formed by oxidizing the upper and side surfaces of the floating gate and the control gate.

75. The semiconductor memory device according to claim 28 further comprising an insulating layer formed on upper and side surfaces of the floating gate and the control gate

wherein said insulating layer is formed by oxidizing the upper and side surfaces of the floating gate and the control gate.

17. 11

76. The semiconductor memory device according to claim 17 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

28. 24. 21

77. The semiconductor memory device according to claim 18 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

41. 39 32 34

78. The semiconductor memory device according to claim 20 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

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62. 64. 46 54 56

79. The semiconductor memory device according to claim 24 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

73. 75. 67 69

80. The semiconductor memory device according to claim 25 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

87. 84 77 80

81. The semiconductor memory device according to claim 26 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

106 110. 100 104

82. The semiconductor memory device according to claim 30 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 1 μm.

83. The semiconductor memory device according to claim 22 wherein a distance between the first and second impurity regions is not larger than 1 μm.

84. The semiconductor memory device according to claim 28 wherein a distance between the first and second impurity regions is not larger than 1 μm.

85. The semiconductor memory device according to claim 17 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.5 μm.

86. The semiconductor memory device according to claim 18 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.5 μm.

87. The semiconductor memory device according to claim 20 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.5 μm.

88. The semiconductor memory device according to claim 24 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.3 μm.

89. The semiconductor memory device according to claim 25 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.3 μm.

90. The semiconductor memory device according to claim 26 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.3 μm.

91. The semiconductor memory device according to claim 30 wherein each distance between the first and second impurity regions and between the first and third impurity regions is not larger than 0.3 μm.

92. The semiconductor memory device according to claim 22 wherein distance between the first and second impurity regions is not larger than 0.3 μm.

93. The semiconductor memory device according to claim 28 wherein a distance between the first and second impurity regions is not larger than 0.3 μm.

94. The semiconductor memory device according to claim 17 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

95. The semiconductor memory device according to claim 18 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

96. The semiconductor memory device according to claim 20 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

97. The semiconductor memory device according to claim 24 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

98. The semiconductor memory device according to claim 26 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

99. The semiconductor memory device according to claim 26 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

100. The semiconductor memory device according to claim 30 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

101. The semiconductor memory device according to claim 22 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

102. The semiconductor memory device according to claim 28 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

103. The semiconductor memory device according to claim 17 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

104. The semiconductor memory device according to claim 18 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

105. The semiconductor memory device according to claim 20 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

106. The semiconductor memory device according to claim 24 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

107. The semiconductor memory device according to claim 26 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

108. The semiconductor memory device according to claim 26 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

109. The semiconductor memory device according to claim 30 wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

110. The semiconductor memory device according to claim 22 wherein a side edge of said floating gate is aligned with a side edge of said control gate.

111. The semiconductor memory device according to claim 28 wherein a side edge of said floating gate is aligned with a side edge of said control gate.

112. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

a third impurity region and a fourth impurity region formed within said semiconductor substrate, wherein said third impurity region is deeper than said fourth impurity region;

wherein said first and third impurity regions are formed in a common impurity region of the semiconductor substrate.

120. 121

113. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region; and

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

a third impurity region and a fourth impurity region formed within said semiconductor substrate, wherein said third impurity region is deeper than said fourth impurity region, wherein said first and third impurity regions are formed in a common impurity region of the semiconductor substrate; and

a pair of wirings formed on and in electrical contact with said second and fourth impurity regions, respectively.

127. 122 126 121

114. The semiconductor memory device according to claim 113 wherein each of said wirings is a bit line.

138. 133

115. A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

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a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

a third impurity region and a fourth impurity region formed within said semiconductor substrate, wherein said third impurity region is deeper than said fourth impurity region, wherein said first and third impurity regions are formed in a common impurity region of the semiconductor substrate;

an interlayer insulating film formed over said semiconductor substrate, said first and second floating gates and said first and second control gates; and

a pair of wirings formed on said interlayer insulating film and electrically connected to said second and fourth impurity regions, respectively, through holes of said insulating film.

116. The semiconductor memory device according to claim 117 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

117. The semiconductor memory device according to claim 118 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

118. The semiconductor memory device according to claim 120 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

119. The semiconductor memory device according to claim 122 wherein the depth of the second impurity region is not larger than 0.1 μm.

120. The semiconductor memory device according to claim 124 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

121. The semiconductor memory device according to claim 125 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

122. The semiconductor memory device according to claim 26 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

123. The semiconductor memory device according to claim 28 wherein the depth of the second impurity region is not larger than 0.1 μm.

124. The semiconductor memory device according to claim 30 wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

125. The semiconductor memory device according to claim 112 wherein the depth of the second and fourth impurity regions is not larger than 0.1 μm.

126. The semiconductor memory device according to claim 113 wherein the depth of the second and fourth impurity regions is not larger than 0.1 μm.

127. The semiconductor memory device according to claim 115 wherein the depth of the second and fourth impurity regions is not larger than 0.1 μm.

128. The semiconductor memory device according to claim 112 wherein said device is an EPROM device.

129. The semiconductor memory device according to claim 113 wherein said device is an EPROM device.

130. The semiconductor memory device according to claim 115 wherein said device is an EPROM device.

131. The semiconductor memory device according to claim 112 wherein said device is an EEPROM device.

132. The semiconductor memory device according to claim 113 wherein said device is an EEPROM device.

133. The semiconductor memory device according to claim 113 wherein said device is an EEPROM device.

134. The semiconductor memory device according to claim 112 wherein said device is a flash memory device.

135. The semiconductor memory device according to claim 113 wherein said device is a flash memory device.

136. The semiconductor memory device according to claim 115 wherein said device is a flash memory device.

137. The semiconductor memory device according to claim 112 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

138. The semiconductor memory device according to claim 113 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

139. The semiconductor memory device according to claim 115 wherein each of said first and second floating gates comprises phosphorus doped polysilicon.

140. The semiconductor memory device according to claim 112 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

141. The semiconductor memory device according to claim 113 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

142. The semiconductor memory device according to claim 115 further comprising an insulating layer formed on upper and side surfaces of the first and second floating gates and the first and second control gates wherein said insulating layer is formed by oxidizing the upper and side surfaces of the first and second floating gates and the first and second control gates.

~~122~~ 117 ~~115~~ 111

143. The semiconductor memory device according to claim 112 wherein each distance between the first and second impurity regions and between the third and fourth impurity regions is not larger than 1 μm.

~~134~~ 129 121 ~~126~~

144. The semiconductor memory device according to claim ~~113~~ wherein each distance between the first and second impurity regions and between the third and fourth impurity regions is not larger than 1 μm.

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~~145~~ 140 121 ~~138~~

145. The semiconductor memory device according to claim ~~115~~ wherein each distance between the first and second impurity regions and between the third and fourth impurity regions is not larger than 1 μm.

~~123~~ 118 ~~115~~ 111

146. The semiconductor memory device according to claim 112 wherein each distance between the first and second impurity regions and between the third and fourth impurity regions is not larger than 0.5 μm.

~~135~~ 130 121 ~~126~~

147. The semiconductor memory device according to claim 113 wherein each distance between the first and second impurity regions and between the third and fourth impurity regions is not larger than 0.5 μm.

~~148~~ 141 121 ~~138~~

148. The semiconductor memory device according to claim ~~115~~ wherein each distance between the first and second impurity regions and between the third and fourth impurity regions is not larger than 0.5 μm.

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